REMARKS/ARGUMENTS

Claims 1-27 remain in the application. Claims 28-30 are cancelled by this amendment. Claims 19-22 are amended to correct informalities.

A. Restriction/Election.

The election of Group I, claims 1-22 is affirmed.

B. Claim Objections.

The amendment to claims 19-22 is believed to overcome the objection raised in the Office Action.

C. Rejections under 35 U.S.C. 112.

Claim 18 was rejected under 35 U.S.C. 112. This rejection is respectfully traversed. At least the implementation described in reference to Fig. 6 teaches an implementation commensurate in scope with claim 18. For example, servo controller 605 implements a physical interface to the data/control bus 602 and a physical interface to the head/actuator mechanism 606. The elements called for by independent claim 1 include a processor 601, data memory 604, a mass storage device formed by the combination of 605/606 and a controller having a memory interface within element 601. It is respectfully requested that the rejection under 35 U.S.C. 112 be withdrawn.

D. Rejections under 35 U.S.C. 102.

Claims 1, 5-11 and 28-31were rejected under 35 U.S.C. 102(b) based upon Tanenbaum. This rejection is respectfully traversed.

Claim 1 calls for, among other things, a controller having a memory interface coupled to the data memory and a mass storage interface coupled to the mass storage device's interface and operable to conduct mass storage transactions between the data memory and the mass storage device. At least this feature of claim 1 is not shown or suggested by Tanenbaum.

Tanenbaum shows a direct memory access (DMA) architecture, but does not show or suggest where the DMA controller is implemented in the system of

Fig 3-3. One can tell that a counter is implemented in memory and DMA registers are implemented in the disk controller, but there is no illustration or discussion of the location of a DMA controller with respect to the CPU, the memory, the disk controller, or the system bus. Tanenbaum's disk controller has only an interface to the system bus, not to a data memory, and so does not satisfy the limitations of the controller called for in claim 1.

Also, there is no hint or suggestion that the disk controller in Tanenbaum would implement a DMA controller, which would more typically be implemented as a subsystem of the CPU or as a chip set coupling the CPU to the system bus. Clearly Tanenbaum shows a highly simplified computer system in Fig. 3-3 that omits fundamental components such as a system chip set and DMA controller. Accordingly, it is questionable whether Tanenbaum is sufficiently accurate and detailed to serve as a basis for rejecting the instant claims.

Claims 5-11 that depend from claim 1 are believed to be allowable for at least the same reasons as claim 1. Further, with respect to claim 6 Tanenbaum does not show a direct memory access controller, so one cannot tell where or how a direct memory access controller might be coupled to the computer system that is shown by Tanenbaum. There is no implication that the DMAC would be coupled in the manner called for in claim 6, nor any motivation to do so. With respect to claims 7-8, the Tanenbaum reference does not describe storage controller processes and application behavior processes implemented using the processor. The illustration on page 92 of Tanenbaum shows a memory map in which memory is allocated to disk tasks, but there is no hint or suggestion that these disk tasks are the same as or similar to the storage controller processes of claim 7 and 8. Similarly, Tanenbaum does not show or fairly suggest a system having the data memory including a logic map of claim 9 or the data structures of claim 10.

Claims 1-4 and 21 were rejected under 35 U.S.C. 102(e) based upon Hunsaker. This rejection is respectfully traversed. Claim 1 calls for, among other things, a controller having a memory interface coupled to the data memory

and a mass storage interface coupled to the mass storage device's interface and operable to conduct mass storage transactions between the data memory and the mass storage device. At least these features of claim 1 are not shown or suggested in the Hunsaker reference.

Hunsaker shows a system in which the mass storage devices couple to the processor through an intermediate mechanism, the ICH 150. Neither the memory controller hub 130 or the ICH 150 have both an interface coupled to the data memory and a mass storage interface. It is not proper to treat the combination of MCH 130 and ICH 150 as a single device as it is core to the Hunsaker device that these elements be implemented as separate devices. As such, they introduce a mandatory interface between the devices that must be traversed by mass storage transactions. The invention of claim 1 eliminates this need for excessive interface traversal and therefore provides an improvement over the architecture of Hunsaker.

Claims 3-4 and 21, which depend from claim 1, are allowable for at least the same reasons as claim 1.

Claims 1, 12, 13 and 20 were rejected under 35 U.S.C. 102(e) based upon Zaidi et al. This rejection is respectfully traversed.

In Fig. 38 Zaidi et al. show a computer architecture in which a bridge device, not a data/control. bus, couples various components. Hence, there is no controller coupled to the CPU bus as called for in claim 1, nor is there a data memory coupled to the processor as called for in claim 1. Instead, the DRAM is coupled to the memory bus (m-bus). Moreover, Zaidi et al, do not teach that the bridge is capable of conduct mass storage transactions between the data memory and the mass storage device. Similarly, Zaidi et al., do not teach that the MAC is capable of conduct mass storage transactions between the data memory and the mass storage device.

Claims 12, 13 and 20, which depend from claim 1, are allowable over Zaidi et al. for at least the same reasons as claim 1.

Claims 1, 14, and 20 were rejected under 35 U.S.C. 102(e) based upon Moriarty et al. This rejection is respectfully traversed.

In Fig. 1 Moriarty et al. show a computer architecture in which a bridge device 106 is required for mass storage transactions. Hence, Moriarty et al. do not show single device a controller that includes both a mass storage interface and an interface to the data memory. Instead, memory controller 108 enables memory transactions between teh processor and the memory, and a separate bridge 106 enables mass storage transactions. Hence, mass storage transactions must traverse multiple interfaces including the SCSI controller, PCI Bus, and Host bus. This multiple bus traversal is minimized in the invention of claim 1.

Claims 14 and 20, which depend from claim 1, are allowable over Moriarty et al. for at least the same reasons as claim 1.

Claims 1, 13-16 and 20-22 were rejected under 35 U.S.C. 102(e) based upon Yiu et al. This rejection is respectfully traversed. The office action relies on Fig. 3 of Yiu et al. to show the specific architecture called for in claim 1. However, Yiu et al. state in paragraph 32 that "...FIG. 3 is not intended to represent any one specific physical arrangement." Accordingly, Fig. 3 does not show a real computer architecture and cannot be relied on to show or suggest the limitations of claims 1, 13-6, and 20-22. Specifically, one cannot, even today, obtain a mass storage device 34 such as a magnetic disk or CDROM that interfaces directly to the same bus as RAM and a processor. Yiu et al. do not identify any such devices and so fail to provide an enabling disclosure of such a system. In contrast, the present invention teaches how to build such a system including such a mass storage device by providing a controller having a memory interface and a mass storage interface. The list of various devices that appears

in paragraph 34 of Yiu et al. describe types of processors, and does not disclose a single device that would show or suggest the controller of claim 1.

Claims 13-16 and 20-22 that depend from claim 1 are distinct over Yiu et al. for at least the same reasons as claim 1.

Claims 1 and 19 were rejected under 35 U.S.C. 102(e) based upon Ellison et al. This rejection is respectfully traversed.

Ellison shows a system in which the mass storage devices couple to the processor through an intermediate mechanism, the ICH 150. Neither the memory controller hub 130 or the ICH 150 have both an interface coupled to the data memory and a mass storage interface. It is not proper to treat the combination of MCH 130 and ICH 150 as a single device as it is core to the Ellison device that these elements be implemented as separate devices. As such, they introduce a mandatory interface between the devices that must be traversed by mass storage transactions. The invention of claims 1 and 19 call for a single controller having a memory interface and a mass storage interface that eliminates this need for excessive interface traversal and therefore provides an improvement over the architecture of Ellison.

Claim 17, which depends from claim 1, was rejected under 35 U.S.C. 102(e) based upon Houston et al. This rejection is respectfully traversed.

Houston shows a computer architecture that lacks a controller having a memory interface and a mass storage interface. North Bridge element 102, by itself, has only a memory interface and a PCI bus interface, not a mass storage interface. Accordingly, Houston does not show or fairly suggest the invention of claim 17.

E. <u>Conclusion.</u>

In view of all of the above, claims 1-27 are believed to be allowable and the case in condition for allowance which action is respectfully requested. Should the Examiner be of the opinion that a telephone conference would

expedite the prosecution of this case, the Examiner is requested to contact Applicants' attorney at the telephone number listed below.

Any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

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Stuart T. Langley, Reg. No. 33,940
Hogan & Hartson LLP
One Tabor Center
1200 17th Street, Suite 1500
Denver, Colorado 80202
(720) 406-5335 Tel
(303) 899-7333 Fax